Tanta University

Department: Physics and Engineering Mathematics
Total Marks: 85 Marks

Faculty of Engineering

Course Title: Engineering Mathematics 3(a) Course Code: PME2109, : PME2110 Year: 2nd
Date: 30/1/ 2022 (First term) Allowed time: 3 hrs No. of Pages: (2)

**Remarks:** (answer the following problems… assume any missing data… answers should be supported by sketches)

## Problem number (1) (40 Marks)

a) Use the values given by $f(x) = x^3 + 2$ at $x = 0, 0.2, 0.4, 0.6, 0.8, \text{and } 1.0$ to find $S_1(x)$ and approximation of $f(x)$ at $x = 0.1, 0.3$ using the Natural Cubic Spline Interpolation.

b) Prove that $f''(x) \simeq \frac{f(x+h) - 2f(x) + f(x-h)}{h^2}$ and $T.E \le \frac{h^2}{12}\left|f^{(4)}(c)\right|, \quad x-h \le c \le x+h$

c) Use Gaussian quadrature (1- midpoint, 2- points, and 3- points) formula to evaluate the integral $I = \int_0^1 \frac{dx}{1+x^2}$ then determine the absolute error.

d) Solve the initial value problem (IVP) by using Euler method $\frac{dy}{dx} = (2x - y), x_o = 0, y_o = -1$. To get the value of (y) at (x=0.5) with (h=0.1) compare the values of the exact solution $y(x) = e^{-x} + 2x - 2$.

## Problem number (2) (45 Marks)

a) Use the Adams third order Predictor Corrector Method to obtain an approximation to the Solution of the initial value problem (IVP) $\frac{dy}{dx} = (2x - y), x_o = 0, y_o = -1$ with (h=0.1) to approximate (y) at (x=0.4)

b) Take the case of a pressure vessel that is being tested in the laboratory to check its ability to withstand pressure. For a thick pressure vessel of inner radius a and outer radius $b$, the differential equation for the radial displacement u of a point along the thickness is given by

$$\frac{d^2u}{dr^2} + \frac{1}{r}\frac{du}{dr} - \frac{u}{r^2} = 0$$

The inner radius $a = 5''$ and the outer radius $b = 8''$. The boundary conditions are:

$$u\big|_{r=a} = 0.0038731''$$

$$u\big|_{r=b} = 0.0030769''$$

Divide the radial thickness of the pressure vessel into 6 equidistant nodes. Solve by using finite difference method. Take $\frac{du}{dr} \approx \frac{u_{i+1} - u_i}{\Delta r}$

c) Find the numerical solution of wave equation $\alpha^2 u_{xx}(x,t) = u_{tt}(x,t), \quad 0 < x < l, \quad 0 < t < T$

Using implicit method.

Where at $j = 0$

$$2u_i^1 - \lambda^2(u_{i+1}^1 - 2u_i^1 + u_{i-1}^1) = 2f_i + 2k\, g_i - k\lambda^2\left(g_{i+1} + 2g_i + g_{i-1}\right)$$

d) Approximate the solution of the wave equation $u_{xx} = u_{tt}$, $0 < x < 1$, $t > 0$ subjected to the initial and boundary conditions:

$u(x,0) = \sin(\pi x), \quad 0 \le x \le 1$

$u_t(x,0) = 0, \quad 0 \le x \le 1$

$u(0,t) = u(1,t) = 0, \quad t > 0$

Use the implicit method with using $h = k = 0.25$

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Dr. Ashraf Al Mahalawy and the committee

Tanta University | **Department: Elec. Computers & Control Engineering** | Faculty of Engineering

Total Marks: 100 Marks

| | | |
|---|---|---|
| Course Title: Data Structures & Algorithms | Course Code: CCE2106 | Year: 2nd |
| Date: 2022 (Final) | Allowed time: 3 Hours | No. of Pages: (4) |

# Model A

**Prove that $9n^2+140n$ is not O(n log n).**

**For sufficiently large n:**

$b\,n^2$ ...(1)... ...(2)... , ...(3)...

$b\,n^2$ + ...(4)... ...(1)... ...(2)... , for all c>0

1) (1) is:
   a) < b) ≥ c) > d) ≤
2) (2) is:
   a) a log n b) $a\,n^2$ c) $a\,n^3$ d) a n log n
3) (3) is:
   a) for all b<0 and a>0 b) for one value b>0 and a<0
   c) for one value b>0 and a>0 d) for all b>0 and a>0
4) (4) is:
   a) c n b) $c\,n^2$ c) c log n d) c n log n

**Complete the following python code of Linear Search for sequence sorted in ascending order:**

```
def orderedSequentialSearch(alist, item):
    for pos in range(len(alist)):
        if alist[pos] = = item:
            ...(1)...
        else:
            if ...(2)... :
                ...(3)...
    ...(4)...
```

5) (1) is:
   a) return False b) return True c) break d) return pos
6) (2) is:
   a) alist[pos] != item b) alist[pos] < item
   c) alist[pos] > item d) none of the above
7) (3) is:
   a) return False b) return True c) break d) return pos
8) (4) is:
   a) return False b) return True c) break d) return pos

**Complete the following function to calculate the multiplication of a list elements:**

```
def listmul(List1):
    if len(List1) = = 1:
        return ...(1)...
    else:
        return ...(2)... * ...(3)... ( ...(4)... )
```



9) (1) is:
   a) List1[0] b) List1[1] c) aList[1] d) none of the above
10) (2) is:
   a) List1[0] b) List1[1] c) aList[1] d) none of the above
11) (3) is:
   a) aList[1] b) aList[2] c) listmul d) none of the above
12) (4) is:
   a) List1[0:] b) List1[1:] c) List1[2:] d) listmul
13) The prefix of the following infix expression A^B-2^5*C is ...
   a) * ^ A B - ^ 2 5 C b) - ^ A B * ^ 2 5 C
   c) A B ^ 2 5 ^ C * - d) ^ A B - * ^ 2 5 C
14) The worst case time complexity of adding an item to unordered linked list = ...
   a) O(n) b) $O(n^2)$ c) O(log n) d) none of the above

**Complete the following function which checks whether the string before % is symmetric to the string after %:**

```
from pythonds.basic.queue import Queue
def is_string_symmetric(input):
    q = Queue( )
    output=[ ]
    for j in range( len(input) ):
        if input[j] != "%":
            ...(1)... ( ...(2)... )
        else:
            break
    for i in range( j+1, len(input) ):
        if ...(3)... ( ) != ...(4)... :
            return not True
    return True
print( is_string_symmetric ("987.65%987.65") )  # return True
print( is_string_symmetric("hello world%helloworld") ) # return False
```

15) (1) is:
   a) q.push b) q.pop c) q.enqueue d) q.dequeue
16) (2) is:
   a) input[j] b) input[i] c) output[j] d) output[i]
17) (3) is:
   a) q.push b) q.pop c) q.enqueue d) q.dequeue
18) (4) is:
   a) input[j] b) input[i] c) output[j] d) output[i]

**Complete the following python code that sorts a linked list data structure:**

```
class Node:
  def __init__(self, initdata):
    self.data = initdata
    self.next = None
  def getData(self):
    return self.data
  def getNext(self):
    return self.next
  def setData(self, newdata):
    self.data = newdata
  def setNext(self,newnext):
    self.next = newnext

class UnorderedList:
  def __init__(self):
    self.head = None
  def add(self,item):
    temp = Node(item)
    temp.setNext(self.head)
    self.head = temp
```

```
def Sort(self):
  i = self.head

  while ...(1)... != None:
      min = ...(2)...
      minposition = i
      j = ...(3)...

      while ...(4)... != None:
        if ...(5)... < ...(6)... :
            min = ...(7)...
            minposition = ...(8)...
        j = ...(9)...

      # Swapping
      temp = ...(10)...
      ...(11)... ( ...(12)... , ...(13)... )
      ...(14)... , ...(15)... ( ...(16)... )

      i = i.getNext( )
```

19) (1) is:
  a) j.getData( )  b) i.getData( )  c) i.setNext( )  d) i.getNext( )
20) (2) is:
  a) j.getData( )  b) i.getData( )  c) i.setNext( )  d) i.getNext( )
21) (3) is:
  a) j.getData( )  b) i.getData( )  c) i.setNext( )  d) i.getNext( )
22) (4) is:
  a) j  b) i  c) j.getNext( )  d) i.getNext( )
23) (5) is:
  a) j.getData( )  b) i.getData( )  c) i.setNext( )  d) i.getNext( )
24) (6) is:
  a) temp  b) min  c) self.head  d) i.getData( )
25) (7) is:
  a) self.head  b) i.getData( )  c) j.getData( )  d) i.getNext( )
26) (8) is:
  a) j  b) i  c) j.getNext( )  d) i.getData( )
27) (9) is:
  a) j  b) i  c) j.getNext( )  d) i.getNext( )
28) (10) is:
  a) min  b) i.getData( )  c) self.head.getData( )  d) j
29) (11) is:
  a) j.setNext  b) j.setData  c) i.setData  d) i.setNext
30) (12) is:
  a) minposition  b) i  c) j  d) temp
31) (13) is:
  a) setNext( )  b) getData( )  c) setData( )  d) getNext( )
32) (14) is:
  a) minposition  b) i  c) j  d) temp
33) (15) is:
  a) getNext  b) getData  c) setNext  d) setData
34) (16) is:
  a) i  b) minposition  c) temp  d) i



**Complete the following python code that inserts a right child to a Binary Tree:**

```
def insertRight( self , value ) :
  if self.right = = None:
    self. ...(1)... = ...(2)... (value)
  else :
    ...(3)... = ...(2)... (value)
    temp.right = self. ...(4)...
    self. ...(5)... = ...(6)...
```

35) (1) is:
  a) left  b) right  c) temp  d) BinaryTree
36) (2) is:
  a) left  b) right  c) temp  d) BinaryTree
37) (3) is:
  a) left  b) right  c) temp  d) BinaryTree
38) (4) is:
  a) left  b) right  c) temp  d) BinaryTree
39) (5) is:
  a) left  b) right  c) temp  d) BinaryTree
40) (6) is:
  a) left  b) right  c) temp  d) BinaryTree

**Complete the following python code that deletes a node with 2 childern from BST:**

```
successor = self. ...(1)... ( ...(2)... )
...(3)... .key = ...(4)... .key
...(3)... .value = ...(4)... .value
...(5)... = self. ...(6)... ( ...(7)... , ...(8)... .key )
return ...(9)...
```

41) (1) is:
  a) bstMaximum  b) bstInsert  c) bstMinimum  d) bstSearch
42) (2) is:
  a) left  b) subtree.right  c) subtree.left  d) subtree
43) (3) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right
44) (4) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right
45) (5) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right
46) (6) is:
  a) bstMaximum  b) bstInsert  c) bstRemove  d) bstSearch
47) (7) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right
48) (8) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right
49) (9) is:
  a) successor  b) subtree  c) subtree.left  d) subtree.right

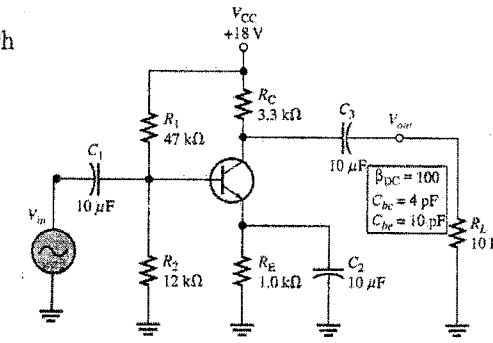
50) In parse tree evaluation, do higher-level subtrees have higher precedence than lower-level subtrees?
  a) Yes  b) No

Tanta University — Electronics and Electrical Communications Department — Faculty of Engineering

| | | | | |
|---|---|---|---|---|
| **Course** | Electronic Circuits and Measurments | **Academic year 2021/2022 First Semester Exam** | **Course Code** | EEC2146 |
| **Year** | $2^{nd}$ Year | | **Total Marks** | 85 |
| **Date** | 26/1/2022 (**Final Exam**) | No. of pages: (4) Pages | **Allowed Time** | 3 hrs |
| **Remarks:** Answer **ALL** the following Questions. | | | | |

## Question # 1: For the Circuit shown below determine: (15) Marks

(a) VB VE Ic VCE Icsat VCE *cutoff* **assume $\beta = 100$**
(b) Draw the Dc load line indicating the position of the Q-point
(c) Draw the AC model;then calculate **Zi, Zo and Av**
(d) The critical frequencies associated with both low and high frequency response
(e) The dominant critical frequencies, the **bandwidth** and **sketch the Bod blot**




## Question # 2: (15) Marks

(a)For the amplifier shown in **Fig.(2-a)** find: $\mathbf{Acl_{(NI)}}$, **Vout , and** $\mathbf{V_f}$
(b) Determine the output voltage for the circuit shown in**Fig.(2-b)** assume $\pm V_{CC} = \pm 15V$
(c) Determine the output voltage of the ideal op-amp shown in **Fig.(2-c)** for the square-wave input shown.

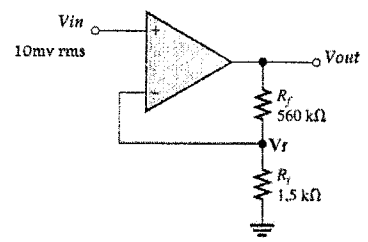



**Fig. (2-a)**

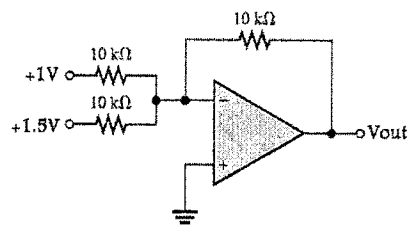



**Fig. (2-b)**

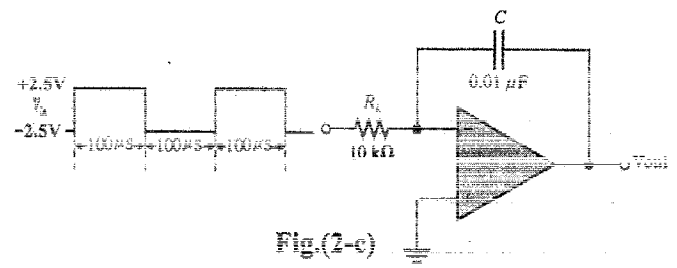
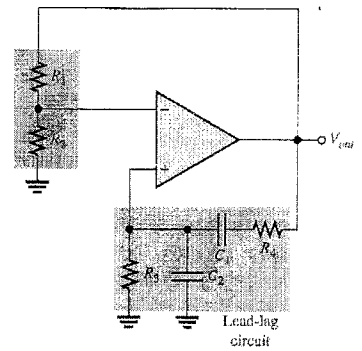



**Fig.(2-c)**



## Question # 3: (10) Marks

For the **Wien-Bridge Oscillator shown below** if R2 = 1kΩ ,R3 =R4 = 10kΩ and C1=C2 = $0.001uf$
(a) Find the value of R1 to **start up** oscillation
(b) Determine the **frequency** of oscillation




## Question # 4: (45) Marks

▪ يتم اجابه هذا الجزء في ورقة التصحيح الالكتروني ولن يلتفت لاي اختيار داخل كراسة الاجابة
▪ الرجاء استخدام القلم الرصاص في الاختيار المبدئي ثم التاكيد في النهاية بالقلم الازرق

*Choose the correct answer*:

1) The maximum value of collector current in a biased transistor is:
(a).IB (b) IC(sat) (c) greater than IE (d) $I_E - I_B$

2) If a sinusoidal voltage is applied to the base of a biased **npn** transistor and the resulting sinusoidal collector voltage is clipped near **saturation** , the transistor is:
(a)operating in linear region (b)operating in cut off (c) operating in saturation (d) Non of the above

3) The disadvantage of base bias is :
(a) very complex (b) produces low gain (c) unstable (d) produces high leakage current

4) If the dc emitter current in a certain transistor amplifier is 3 mA, the approximate value of $r_e$ is:
(a) $3k\Omega$ (b) $3\Omega$ (c) $8.66\Omega$ (d) $0.66k\Omega$

5) certain common-emitter amplifier has a voltage gain of 100. If the emitter bypass capacitor is removed,:
(a) the circuit will become unstable (b) the voltage gain will decrease
(c) the voltage gain will increase (d) the Q-point will shift

6) For a common-emitter amplifier,Rc =1kΩ, $RE = 390\Omega, re = 15\Omega and \beta = 75$. Assuming that RE is **completely bypassed** at the operating frequency, the voltage gain is:
(a) -66.66 (b) -2.56 (c) -2.47 (d) -75

7) If a 10 mV signal is applied to the base of the **emitter-follower** , the output signal is approximately:
(a) 100 mV (b) 150 mV (c) 1.5 V (d) 10 mV

8) If each stage of a **four-stage amplifier** has a voltage gain of 15. The overall voltage gain is:
(a) 60 (b) 15 (c) 50,625 (d) 3078

9) The overall gain found in Question 8 can be expressed in decibels as:
(a) 94.1 dB (b) 47.0 dB (c) 35.6 dB (d) 69.8 dB

10) A bypass capacitor in a CE amplifier decreases the voltage gain :
(a) True (b) False (c) Non of the above (d) a&b

11) If RC in a CE amplifier is increased, the voltage gain is reduced
(a) True (b) False (c) Non of the above (d) a&b

12) A CC amplifier has high voltage gain
(a) False (b)Non of the above (c) True (d) a&b

13) Internal transistor capacitance has no effect on an amplifier's frequency response
(a) True (b) False (c) Non of the above (d) a&b

14) A ten-times change in frequency is called a decade
(a) True (b) False (c) Non of the above (d) a&b

15) Bypass capacitors in an amplifier determine the high-frequency response.
(a) True (b) False (c) Non of the above (d) a&b

16) The Miller input capacitance of an amplifier is dependent, in part, on:
(a) the input coupling capacitor (b) the voltage gain (c) the bypass capacitor (d) none of these

17) The decibel is used to express:
(a) power gain (b) voltage gain (c) attenuation (d) all of these

18) In an amplifier, the gain that occurs between the lower and upper critical frequencies is called the:
(a) critical gain (b) midrange gain (c) bandwidth gain (d) decibel gain

19) At the upper critical frequency, the peak output voltage of a certain amplifier is 10 V. The peak voltage in the midrange of the amplifier is:
(a) 7.07 V (b) 6.37 V (c) 14.14 V (d) 10 V

20) The Miller input and output capacitances for a BJT inverting amplifier depend on:
(a) Cbc (b) $\beta$ (c) Av (d) answers (a)& (c)

21) The bandwidth of an amplifier is determined by:
(a) the midrange gain (b) the critical frequencies (c) the roll-off rate (d) the input capacitance

22) An amplifier has the following critical frequencies: 1 kHz, 950 Hz, 8 MHz, and 10 MHz. The bandwidth
(a) 7999 Hz (b)9999 Hz (c) 7.99 MHz (d) 9.99 MHz

23) Ideally, the midrange gain of an amplifier:
(a) increases with frequency (b) decreases with frequency (c) remains constant with frequency (d) depends on the coupling capacitors

24) An ideal op-amp has an infinite input impedance.
(a) True (b) False (c) Non of the above (d) a&b

25) An ideal op-amp has a very high output impedance
(a) True (b) False (c) Non of the above (d) a&b

26) Negative feedback reduces the gain of an op-amp from its open-loop value.
(a) True (b) False (c) Non of the above (d) a&b

27) If the feedback resistor in an inverting amplifier opens, the gain becomes zero
(a) True (b) False (c) Non of the above (d) a&b

28) When an op-amp is operated in the single-ended differential mode,
(a) the output is grounded (b) one input is grounded and a signal is applied to the other
(c) both inputs are connected together (d) the output is not inverted

29) In the common mode,
(a) both inputs are grounded (b) the outputs are connected together
(c) an identical signal appears on both inputs (d) the output signals are in-phase



30) The use of negative feedback
(a) reduces the voltage gain of an op-amp (b) makes the op-amp oscillate
(c) increase the voltage gain of an op-amp (d) answers (a) and (b)

31) A certain noninverting amplifier has an Ri of 1k$\Omega$ and an Rf of 100k$\Omega$ The closed-loop gain is
(a) 100,000 (b) 1000 (c) 101 (d) 100

32) If the feedback resistor in Question 30 is open, the voltage gain
(a) increases (b) decreases (c) is not affected (d) depends on Ri

33) A summing amplifier can have more than two inputs
(a) True (b) False (c) Non of the above (d) a&b

34) A summing amplifier can have:
(a) only one input (b) only two inputs (c) any number of inputs

35) An averaging amplifier has five inputs. The ratio Rf/Ri must be:
(a) 5 (b) 0.2 (c) 1 (d) 0.5

36) When you apply a triangular waveform to the input of a differentiator, the output is:
(a) a dc level (b) an inverted triangular waveform
(c) a square waveform (d) the first harmonic of the triangular waveform

37) Positive feedback is used in oscillators.
(a) True (b) False (c) Non of the above (d) a&b

38) For start-up, the loop gain must be greater than 1
(a) True (b) False (c) Non of the above (d) a&b

39) ..... are Used to generate clocks in digital systems
(a) filters (b) oscillators (c) transducers (d)batteries

40) An oscillator differs from an amplifier because the oscillator
(a) has more gain (b) requires no input signal (c) requires no dc supply (d) always has the same output

41) One condition for oscillation is :
(a) a phase shift around the feedback loop of 180° (b) a gain around the feedback loop of one-third
(c) a phase shift around the feedback loop of 0° (d) a gain around the feedback loop of less than 1

42) A second condition for oscillation is:
(a) no gain around the feedback loop (b) a gain of 1 around the feedback loop
(c) the attenuation of the feedback circuit must be one-third (d) the feedback circuit must be capacitive

43) The Wien-bridge oscillator's positive feedback circuit is:
(a) an RL circuit (b) an LC circuit (c) a voltage divider (d) an RC circuit

44) In a Wien-bridge oscillator, if the resistances in the positive feedback circuit are decreased, the frequency:
(a) decreases (b) increases (c) remains the same

45) In a certain oscillator,Av=50. The attenuation of the feedback circuit must be
(a) 1 (b) 0.01 (c) 10 (d) 0.02

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Good Luck

Course Coordinator: *Dr.Nessim Mahmoud*

Tanta University | Department: Computer and Automatic Control Engineering | Faculty of Engineering

Total Marks: 75 Marks

| | | |
|---|---|---|
| Course Title: **Microprocessors and Interfacing Systems** | Course Code: CCE2108 | Year: 2nd |
| Date: 12/01/2022 | Allowed Time: 3 hours | **Model A** |

**Answer ALL the following questions.**

## Question (1) Choose the correct answer (40 Marks)

**1)** _____ are the registers that cannot be addressed directly by a program.

a. Program visible registers.
b. Program invisible registers.
c. Segment registers.
d. None of the above.

**2)** Intel 8086/8088 microprocessor address bus can locate

a. 1024 locations
b. 524,288 locations
c. 1,048,576 locations
d. 2,097,152 locations

**3)** Which of the following instructions is used to transfer a byte, word, or doubleword of data from data segment memory location to an I/O device?

a. INS b. OUTS c. STOS d. LODS

**4)** The 1 MB byte of memory can be divided into segment

a. 1 Kbyte b. 64 Kbyte c. 33 Kbyte d. 34 Kbyte

**5)** If the clock of 8086/8088 is operated at 10 MHz, how long is one bus cycle?

a. 800 ns b. 1600 ns c. 400 ns d. 200 ns

**6)** In max mode, control bus signal So,S1 and S2 are sent out in ..... form.

a. decoded b. encoded c. shared d. unshared

**7)** Access time is faster for .....

a. ROM b. SRAM c. DRAM d. EEPROM

**8)** Which of the following is not an arithmetic instruction?

a. INC b. CMP c. DEC d. ROL

**9)** Number of the times the instruction sequence below will loop before coming out of loop is:

```
      MOV CL, 00h
Again: INC CL
      JNZ Again
```

a. 0 b. 1 c. 255 d. 256 e. 254



**10)** In 8086 microprocessor one of the following statements is not true.

a. Coprocessor is interfaced in MAX mode.
b. Coprocessor is interfaced in MIN mode.
c. I/O can be interfaced in MAX/MIN mode.
d. Memory can be interfaced in MAX/MIN mode.

**11)** Which of the following components should be connected to the Microprocessor to be able to connect its output pin to more than 10 loads?

a. Latch b. Multiplexer c. Buffer d. Decoder

**12)** How can we sum the following two 16-bit numbers using Intel 8086 Microprocessor:
(2FB1) + (A23E)

a. Use single ADD instruction
b. Use ADD instruction followed by ADC instruction
c. Use two sequential ADD instructions
d. Use ADC instruction followed by ADD instruction
e. Use XADD instruction

**13)** Which of the following instruction is not valid?

a. MOV AX, BX
b. MOV ES, 5000H
c. MOV AX, 5000H
d. PUSH AX

Determine the address of the memory locations accessed by the following instructions **(Questions 14, 15, 16, and 17)**, assume real-mode memory addressing.

**Suppose that:**

| | | | |
|---|---|---|---|
| EAX | | 10 | 10 |
| EBX | | 20 | 40 |
| | | | |
| ESI | | 00 | 20 |
| EDI | | 00 | 30 |
| ESP | | 00 | 10 |

| | |
|---|---|
| **CS** | **0100** |
| **DS** | **0200** |
| **SS** | **0300** |
| **EX** | **0400** |

**14)** MOV AX, ARRAY[DI] **[Note: ARRAY = 2000H]**

a. 5000 H, 5001 H
b. 5030 H, 5031 H
c. 4030 H, 4031 H
d. 5030 H

**15)** MOV AX, [BX]

a. 4020 H
b. 2040 H
c. 4040 H, 4041 H
d. 4040 H
e. 2040 H, 2041 H

**16)** JMP AX

a. 2010 H
b. 1010 H
c. 3010 H
d. 2010 H, 2011 H
e. 1010 H, 1011 H

**17)** MOV EAX, [BX + SI + 300H]

a. 4240 H, 4241 H
b. 4240 H, 4241 H, 4242 H, 4243 H
c. 4360 H, 4361 H, 4362 H, 4363 H
d. 2240 H, 2241 H

---

**18)** During the execution of an interrupt, which of the following registers are pushed into the stack:

1) IP 2) Flag Register 3) DS 4) CS 5) SP

a. 1 & 2 b. 1 & 2 & 3 c. 1 & 2 & 3 & 4 d. 1 & 2 & 4 e. 1 & 2 & 4 & 5

**19)** Intel 8086 microprocessor, READY signal used

a. To indicate to user that the microprocessor is working and is ready for use.
b. To slow down a fast peripheral device so as to communicate at the microprocessor's device.
c. To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.
d. None of the above.

**20)** Consider the following statements: In 8086 microprocessor, data-bus and address bus are multiplexed in order to

I) Increase the speed of microprocessor.
II) Reduce the number of pins.
III) Connect more peripheral chips.

Which of these statements is/are correct?

a. (I) only
b. (II) only
c. (II) & (III)
d. (I), (II) & (III)

---



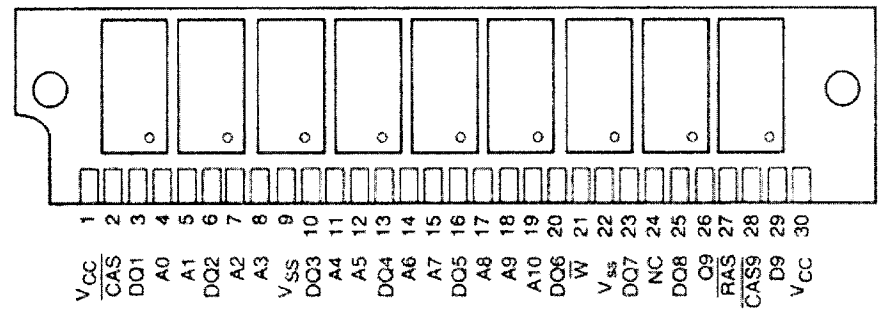
## Question (2) (15 Marks)

A. What is the difference between real-mode memory addressing and protected-mode memory addressing? Explain briefly the operation of each mode. **(5 Marks)**

B. Consider the two registers **EAX** and **EBX** which contain initial values **2FA1 9B8D**H, and **1EA3 4EF1**H respectively. Write the value of **EBX** register after executing each of the following operations **separately**: **(5 Marks)**

a. MOV AL, BL
b. MOV BH, AH
c. MOV BX, AX
d. MOV EBX, EAX
e. INC BX

C. For the illustrated 30-pin SIMM, answer the following questions: **(5 Marks)**




a. Describe the pinout of the illustrated 30-pin SIMM. **(2 Marks)**

b. Determine the capacity of the illustrated 30-pin SIMM in terms of (**n** locations × **b** bits). **(2 Marks)**

c. What does DDR stand for? What does it technically mean? **(1 Marks)**

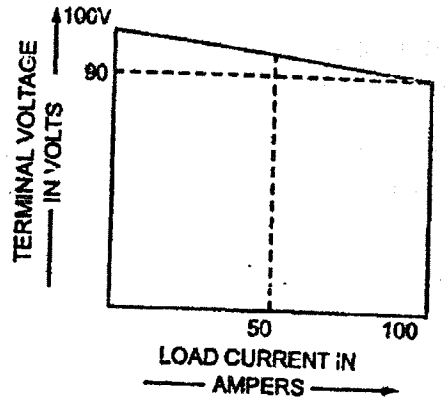
## Question (3) (20 Marks)

A. Design a memory interface for a 8086 microprocessor to connect it to **eight** EPROMs, 64K × 8 memory devices to form a total memory of 512K × 8 bits of the physical address space of the microprocessor starting from memory address **20000H** to memory address **9FFFFH**. **Draw your design with illustrating the used electronic components, address and data bus connections and determine the address range for each EPROM.** **(10 Marks)**

B. Write a 8086 assembly programs to find the **sum of numbers** in a block of data consists of (14) byte-wide numbers stored at memory starting from memory address AD10H to memory address AD1DH. Store the sum in location B000H. **(10 Marks)**

*Best Wishes,*
*Dr. Amr Elkholy*

| | |
|---|---|
| B | The external load characteristic of a dc generator at rated speed is assumed to be linear and is shown in the figure. The load circuit comprises only resistance. **[6 Marks]** |



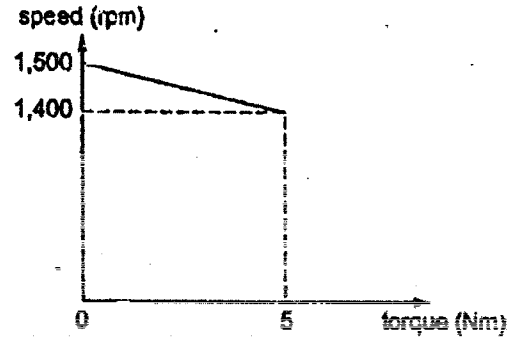

**Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (ورقة التصحيح الإلكتروني).**

26. When the load current is 50 A, the value of armature resistance is
(a) 0.9 Ω (b) 0.1 Ω (c) 1.9 Ω (d) 2.0 Ω

27. The generated *emf* at 75 A will equal
(a) 115 V (b) 90 V (c) 100 V (d) 85 V

28. The value of load circuit resistance when the load current is 25 A will be
(a) 1.9 Ω (b) 3.9 Ω (c) 0.1 Ω (d) 1.23 Ω

| | |
|---|---|
| C | A separately excited DC motor runs at 1500 rpm under no load with 200 V applied to the armature. The field voltage is maintained at its rated value. The speed of the motor, when it delivers a torque of 5 Nm, is 1400 rpm as shown in the figure. The rotational losses and armature reaction are neglected. **[6 Marks]** |




**Solve the above problem to determine the following, then choose the closest answer and put it in the answer sheet (ورقة التصحيح الإلكتروني).**

29. The back *emf* when the motor runs at 1400 rpm would be
(a) 175 V (b) 213.3 V (c) 186.67 V (d) 200 V

30. The armature resistance of the motor is
(a) 2 Ω (b) 3.4 Ω (c) 4.4 Ω (d) 7.7 Ω

31. For the motor to deliver a torque of 2.5 Nm at 1400 rpm, the armature voltage to be applied is
(a) 125.5 V (b) 193.3 V (c) 200 V (d) 241.7 V





| | |
|---|---|
| D | A 9kVA, 208V, 1200rpm, 3-phase, 60Hz, star connected, synchronous generator with a field winding resistance of 4.5Ω. The armature winding impedance is 0.3+j5 Ω/phase. When the generator operates at its full load and 0.8 pf lagging, the field winding current is 5A. The rotational loss is 500W. **Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (ورقة التصحيح الإلكتروني).** **[6 Marks]** |

32. The voltage regulation is
(a) 47.22% (b) 37.8% (c) 85% (d) -5.88%

33. The efficiency of the generator is
(a) 68.5% (b) 86% (c) 89% (d) Leadscrew

34. The torque applied by the prime mover is.
(a) 103N.m. (b) 55N.m. (c) 35N.m. (d) 67N.m.

| | |
|---|---|
| E | A 3-phase, 20hp, 500V, 50Hz, 6-pole, star connected induction motor running at 950rpm with 0.85 lagging power factor. The mechanical losses are 1hp, the stator copper losses are 1500W, while the core losses are 500W. **Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (ورقة التصحيح الإلكتروني).** **[6 Marks]** |

35. The rotor copper loss is
(a) 635.5W (b) 412.5W (c) 825W (d) 1000W

36. The line current is
(a) 25A (b) 50A (c) 57.013A (d) 7.47A

37. Motor efficiency is.
(a) 76.96% (b) 81% (c) 87.31% (d) 95%

## The second question (9 marks)

| | |
|---|---|
| A | **Explain**, *with all necessary equations and figures*, the terminal characteristic of a series DC generator. |
| B | **What** could be wrong if a shunt generator is started and no voltage builds up? |
| C | **Explain** the various speed control methods of shunt DC motors. |

## The third question (12 marks)

| | |
|---|---|
| A | Draw the torque-speed curve of 3-phase induction motor and indicate points of interest on it. |
| B | List the different types of single-phase induction motor. |
| C | State the advantages of different types of stepper motors. |

***Wish you all best wishes.***

*Dr. Ahmed Elrefaie*

*Dr. Mohamed Gamal Hussien*

**Final EXAM 2021/2022 - First Term**

| | | | |
|---|---|---|---|
| Course | Energy conversion (EPM2143) | Time | 3 hours |
| Students | 2nd Year (Computer and Control Engineering) | Mark | 70 |
| Date | 23 / 1 /2022 | No. of pages | 4 |

*Answer ALL the following questions:*

## The first question (49 marks)

**A** **Choose the correct answer and put it in the answer sheet(ورقة التصحيح الإلكتروني). [25Marks]**

1. The rotor of a stepper motor has NO
(a) Windings (b) Commutator (c) Brushes (d) All of the mentioned

2. Which of the following is NOT a type of stepper motor?
(a) Variable Reluctance (b) Hybrid (c) Magnetic (d) Leadscrew

3. 3-phase induction motor if runs above Synchronous Speed runs as:
(a) Induction Generator (b) Synchronous Generator (c) Synchronous Motor (d) reactor

4. Which of the following phase sequence represents half-step operation of a VR stepper motor?
(a) A, B, C, A (b) A, C, B, A (c) AB, BC, CA, AB (d) A, AB, B, BC

5. Slip of 3-Phase Induction Motor should always be.
(a) Greater than one (b) Equal to one (c) Zero (d) Less than one

6. A Synchronous Machine having 8 poles and supplied with 50 Hz supply will rotate at.
(a) 1500 rpm (b) 1800 rpm (c) 3000 rpm (d) 750 rpm

7. The Poles and Pole Shoes of a Synchronous Machine is laminated to reduce:
(a) Hysteresis Loss (b) Eddy Current Loss (c) Armature Reaction (d) Stray losses

8. Which one of the following motors is not self-starting?
(a) 3-ph induction (b) Dc motor (c) Servo motor (d) Synchronous

9. Starting Currents of 3-Phase Induction Motor is about ____ times of the full load current:
(a) 10 to 20 (b) Half (c) 5 to 7 (d) 2 to 3

10. 3-Phase Induction Motor will have ____ Starting Torque and _____ Starting Current.
(a) Low, Low (b) High, Low (c) High, High (d) Low, High

11. Wave winding is employed in a dc machine of
(a) high current and low voltage rating (c) high current and high voltage rating
(b) low current and high voltage rating (d) low current and low voltage rating

12. A lap wound dc machine has 400 conductors and 8 poles. The voltage induced per conductor is 2 V. The machine generates a voltage of
(a) 100 V (b) 200 V (c) 400 V (d) 800 V

13. The armature resistance of a 6-pole lap wound dc machine is 0.05 Ω. If the armature is rewound as a wave winding, what is the armature resistance?
(a) 0.45 Ω (b) 0.30 Ω (c) 0.15 Ω (d) 0.10 Ω





14. When the shunt filed of a dc compound generator is connected across both the series field and armature. Such a connection is known as
(a) short shunt (b) long shunt (c) cumulative compounding (d) differential compounding

15. The voltage at the terminals of a dc series generator running at rated rpm and no load will be
(a) more than the rated voltage (b) full rated voltage (c) a very small voltage (d) zero

16. A dc shunt generator is supplying a load of 1.8 kW at 200 V. Its armature and field resistances are 0.4 Ω and 200 Ω, respectively. What is the generated *emf*?
(a) 190 V (b) 196 V (c) 204 V (d) 210 V

17. If the filed circuit resistance of a dc shunt generator exceeds its critical value, the generator
(a) fails to build up (c) exceeds its current capacity
(b) builds up a very high voltage (d) produces power beyond its rating

18. Which of the following dc generators will have negligible terminal voltage on no load?
(a) Shunt (b) Series (c) Compound (d) None

19. 3-Phase Induction Motor will have ____ Starting Torque and _____ Starting Current. A 220 V dc machine has an armature resistance of 1 Ω. If the full-load current is 20 A, the difference of induced voltage, when the machine is running as a motor and generator, is
(a) 20 V (b) Zero (c) 40 V (d) 60 V

20. A dc shunt motor runs at rated speed. If its filed circuit gets open circuited, then soon after the motor speed will
(a) decrease (b) remain unchanged (c) increase (d) None of the above

21. What is the increase in torque expressed as percentage of initial torque, if the current drawn by a dc series motor is increased from 10 A to 12 A (neglect saturation)?
(a) 21 % (b) 25 % (c) 41 % (d) 44 %

22. A 200 V, 2000 rpm, 10 A, separately excited dc motor has an armature resistance of 2 Ω. Rated dc voltage is applied to both the armature and field windings of the motor. IF the armature draws 5 A, from the source, the torque developed by the motor is
(a) 4.30 Nm (b) 4.77 Nm (c) 0.45 Nm (d) 0.50 Nm

23. The speed of a 4-pole dc series motor at no load will be
(a) zero (b) 3000 rpm (c) infinite (d) 1500 rpm (e) depending upon the applied voltage

24. If the speed of a dc motor increases with load torque, then it is a
(a) series motor (c) differentially compounded motor
(b) permanent magnet (d) cumulatively compounded motor

25. A dc shunt motor is driving a constant torque load with normal excitation. If the filed current is halved, then the motor will run at
(a) rated speed (c) double of rated speed
(b) half of rated speed (d) slightly less than double the rated speed

Model (A)

Tanta University

**Department:** Computers and Control Eng.
**Total Marks: 75** Marks
**Academic Year: 2021/2022(First Semester)**

Faculty of Engineering

Course Title: **Digital Systems** Course Code: **CCE2107** **Second Year Students**
Date: **16-1-2022 (End-of-Semester Exam)** **Model (A)** Time Allowed: **3 hours** No. of Pages: **(4)**

**Answer all the following questions.**

**Question (1)** **(75 Points)**

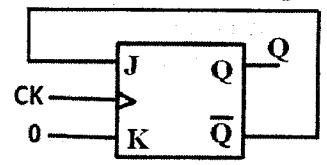
**Shade the circle of the most appropriate answer in your electronic answer sheet:**

1) When designing a synchronous counter with D flip-flops (Inputs: $D_A$, $D_B$, and $D_C$ /Outputs: A (least significant bit), B, and C (most significant bit)) that goes through the following binary repeated sequence: 0, 4, 1, 6, 0,… . (Hint: Use Karnaugh map to get the simplest form of flip flops input equations); Binary states 010, 011, 101 and 111 are considered as don't care conditions (unused states). If the counter goes to the state 101, the next state will be:
a) 010 b) 100 c) 000 d) 011 e) None of these
2) Consider the counter in **(point )**, the input of the first flip-flop A is
a) $D_A$=A.C b) $D_A$=B c) $D_A$=B'.C d) $D_A$=C e) None of these
3) Consider the counter in **(point )**, the input of the second flip-flop B is
a) $D_B$=A.C b) $D_B$=A c) $D_B$=A'.C d) $D_B$=C e) None of these
4) Consider the counter in **(point )**, the input of the third flip-flop C is
a) $D_C$=A.B b) $D_C$=A c) $D_C$=C' d) $D_C$=B.C e) None of these
5) Consider the counter in **(point )**, If the counter goes to the state 111, the next state will be:
a) 010 b) 100 c) 001 d) 000 e) None of these
6) Consider the counter in **(point )**, The number of stuck states is:
a) Zero b) 1 c) 2 d) 3 e) None of these
7) A MOD-5 ripple counter uses a flip-flop with propagation delay of 20 ns. The pulse width of strobe is 30ns. The frequency of input signal which can be used for proper operation of counter is?
a) 8 MHz b) 13 MHz c) 20 MHz d) 22 MHz e) None of these
8) For a MOD-12 ripple counter, the flip-flop has a propagation delay = 60 ns and the NAND gate has a propagation delay of 25 n sec. The max. clock frequency that can be used is equal to
a) 3.77 MHz b) 4.87 MHz c) 1.34 MHz d) None of these
9) Asynchronous counters eliminate the …… problems encountered with synchronous counters.
a) delay b) stuck c) race around d) None of these
10) The minimum number of D flip-flops needed to design a mod-258 counter is.
a) 9 b) 8 c) 7 d) 258 e) None of these
11) Three cascaded D flip-flop will divide the input frequency by _____.
a) 3 b) 6 c) 8 d) None of these
12) The terminal count of a modulus-11 binary counter is _____.
a) 1010 b) 1011 c) 1001 d) 1100 e) None of these
13) Mealy machine has _____ states than a Moore machine.
a) Fewer b) More c) Equal d) Negligible e) None of these
14) Conditional box has a shape of
a) square b) rectangle c) oval d) pentagon e) None of these
15) What is a square wave generator?
a)Bistable multivibrator b)Astable multivibrator c)Monostable multivibrator d) None of these
16) …… is useful for creating a timing period of fixed duration in response to some external event.
a) Astable Multivibrator b) Monostable Multivibrator c) Bistable Multivibrator d)None of these
17) Which of the following conditions must be met to avoid race around problem.
a) Pulse width < Propagation delay b) Pulse width >Propagation delay c) None of these
18) Race around problem is unwanted and uncontrollable oscillations occurring in ……
a) Pulse-triggered JK b) Edge-triggered JK c) All of these d) None of these

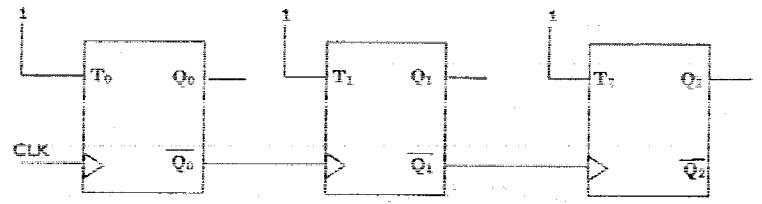




19) The state diagram to describe a sequence detector using a Moore machine that detects three consecutive 0's or three consecutive 1's with overlapping includes at maximum:
a) 4 states b) 5 states c) 6 states d) 7 states e) None of These
20) A sequence detector is designed to detect precisely 3 digital inputs, without overlapping sequences detectable. For the sequence (1X1) and input data (110101001111010): what is the output of this detector?
a) 000101000011110 b) 000101000010110 c) 000001000010010 d) None of These
21) A sequence detector using a Mealy machine is required to give a logical output of 1 whenever the sequence 11010001 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is
a) 8 b) 5 c) 4 d) 3 e) None of These
22) The state diagram to describe a sequence detector using a Moore machine that accept a string containing even number of zeros:
a) 2 states b) 3 states c) 4 states d) 5 states e) None of These
23) The output of a 5-input AND gate is connected to the input of 2 gates, this gate has a fan-out of……
a) 2 b) 3 c) 4 d) 5 e) None of the mentioned
24) The output of a 2-input AND gate is connected to the input of 5 gates, this gate has a fan-in of ……
a) 2 b) 3 c) 4 d) 5 e) None of the mentioned
25) How many pulses are needed to change the contents of a 4-bit down counter from 1100 to 0111 (rightmost bit is the LSB)?
a) 4 b) 5 c) 6 d) 7 e) None of these
26) The number of unused states in the 6-bit Johnson counter is:
a) 6 states b) 32 states c) 64 states d) None of these
27) In a JK flip-flop, we have J=Q' and K=0 (see figure). Assuming the flip-flop was initially with Q=1 and then clocked for 6 pulses, the next sequence at the Q output will be

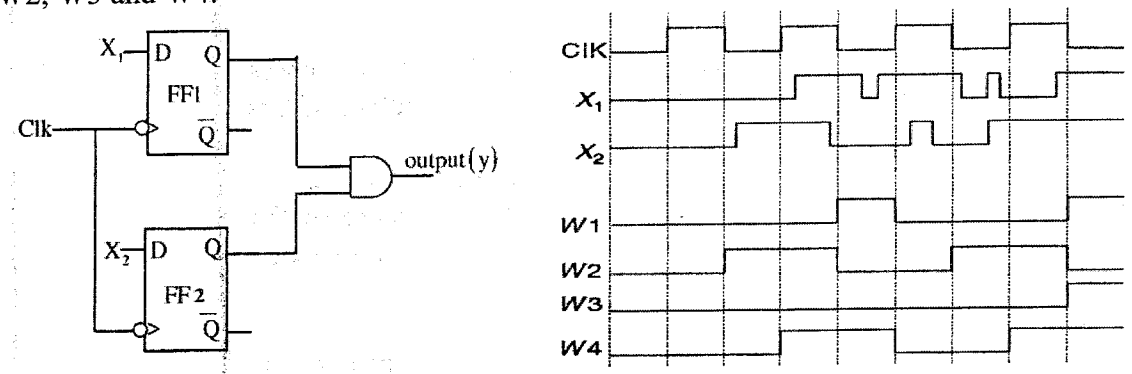



a) 101010 b) 000000 c) 111111 d) 010101 e) None of these
28) Assume that a four-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the four-bit pattern after the fourth clock pulse? (Right-most bit first.)
a) 1111 b) 1100 c) 0000 d) 0011 e) None of these
29) In a 3-bit Johnson counter sequence, there are a total of how many states or bit patterns?
a) 6 b) 8 c) 3 d) 10 e) None of these
30) Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-$2^n$ bit decoder. This circuit is equivalent to a ……..
a) k-bit ring counter. b) 2k-bit ring counter. c) k-bit Johnson counter. d) None of these
31) The given figure shows a ripple counter using positive edge triggered flip flops. If the present state of the counter is $Q_0\ Q_1\ Q_2 = 110$, then its next state $Q_0\ Q_1\ Q_2$ will be



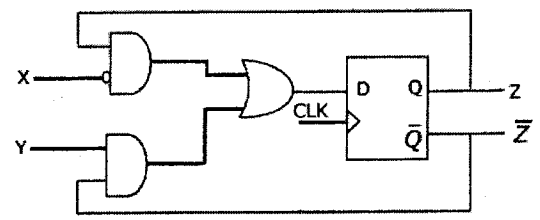

a) 010 b) 001 c) 111 d) 101 e) None of these
32) Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is:
a) 0, 1, 3, 7, 15, 14, 12, 8, 0 b) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
c) 0, 8, 12, 6, 8, 10, 12, 1, 0 d) 0, 8, 12, 14, 15, 7, 3, 1, 0 e) None of these

33) In the circuit shown, choose the correct timing diagram of the output (y) from the given waveforms W1, W2, W3 and W4.



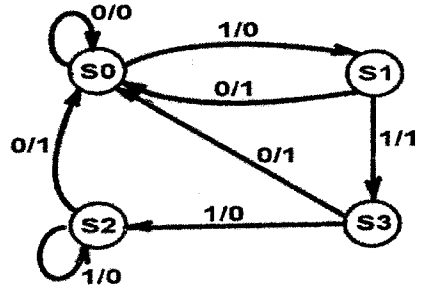

a) W1 b) W2 c) W3 d) W4 e) None of these

34) A sequential circuit using D flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is




a) S–R Flip-Flop with inputs X = R, Y = S b) J–K Flip-Flop with inputs X = S, Y = R
c) J–K Flip-Flop with inputs X = K, Y = J d) None of these

35) What is the number of states obtained after minimizing the given state graph shown in figure?
a) 2 b) 3 c) 4 d) None of these



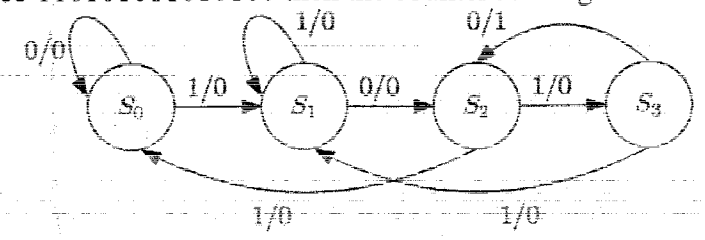

36) Consider the state graph in **(point 35)**, what is the minimum number of flip-flops needed to build the equivalent circuit for the state graph after minimization?
a) 1 b) 2 c) 3 d) 4 e) None of these

37) To convert D flip-flop to JK flip-flop:
a) D=J'.Q+Q'.K b) D= J.Q'+Q'.K c) D= J.Q'+Q.K' d) None of these

38) Assume a 4-bit ripple counter has a failure in the second flip-flop such that it "locks up". The third and fourth stages will _____
a) Continue to count with correct outputs b) Turn into molten silicon
c) Continue to count but have incorrect outputs d) Stop counting e) None of these

39) A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is…
a) constantly LOW b) constantly HIGH
c) a 20 kHz square wave d) a 10 kHz square wave e) None of these

40) The given figure shows the state graph of a sequence detector machine. The output of machine is connected to a decimal counter that increments whenever the output goes high. If the input to the machine is the sequence 110101011010100 then the counter reading after the end of sequence is

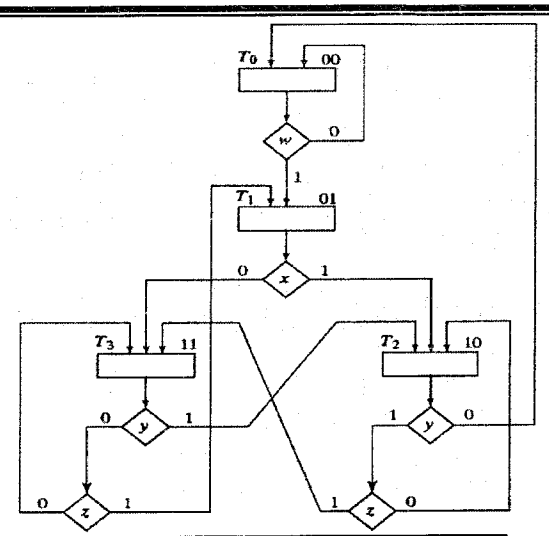



a) 2 b) 3 c) 4 d) 5 e) None of these





**Taking into consideration the algorithmic state machines chart shown in figure, solve the questions from (point 41) to (point 44)**




41) How many states in the chart?
a) 2 b) 3 c) 4 d) 6 e) None of these

42) How many blocks in the chart?
a) 6 b) 4 c) 3 d) 2 e) None of these

43) How many inputs are required for the control logic part?
a) 6 b) 4 c) 3 d) 2 e) None of these

44) What is the minimum number of flip-flops needed to build the control logic part?
a) 4 b) 3 c) 2 d) 1 e) None of these

45) Which of the following is the Universal Flip-flop?
a) S-R flip-flop b) J-K flip-flop c) D Flip-flop d) None of these

46) In DOWN-counter, each flip-flop is triggered by the …….. of the preceding flip-flop
a) inverted output ($Q^{\backslash}$) b) output (Q) c) input d) None of these

47) In asynchronous circuit, the changes occur with the change of
a) input b) output c) clock pulse d) time e) None of these

48) Hold time is defined as the time required for the data to _____ after the triggering edge of clock.
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49) An 8-bit serial in/serial out shift register is used with a clock frequency of 200 kHz to achieve a time delay (td) of _____
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55) In VHDL, Bus is a type of _____
a) Signal b) Constant c) Variable d) Driver e) None of these

56) STD_LOGIC data type can have the value?
a) X b) Z c) 0 d) All of these

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60) In VHDL, which of the following can be the name of an entity?
a) entity_2 b) 2 entity c) entity d) All of these e) None of these

**End of questions** **BEST WISHES**

**Course Instructor:** Dr. Mohamed Abdalla Attia

Tanta University — **Department:** Computers and Control Eng. — **Faculty of Engineering**

**Total Marks: 75** Marks

**Academic Year: 2021/2022(First Semester)**

Course Title: **Digital Systems** Course Code: **CCE2107** **Second Year Students**

Date: **16-1-2022 (End-of-Semester Exam)** Model (B) Time Allowed: **3 hours** No. of Pages: **(4)**

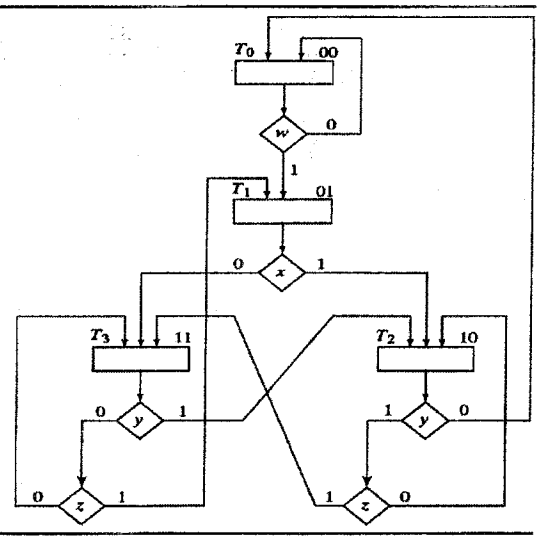
**Answer all the following questions.**

**Question (1)** **(75 Points)**

**Shade the circle of the most appropriate answer in your electronic answer sheet:**

1) When designing a synchronous counter with D flip-flops (Inputs: $D_A$, $D_B$, and $D_C$ /Outputs: A (least significant bit), B, and C (most significant bit)) that goes through the following binary repeated sequence: 0, 4, 1, 6, 0,… . (Hint: Use Karnaugh map to get the simplest form of flip flops input equations); Binary states 010, 011, 101 and 111 are considered as don't care conditions (unused states). If the counter goes to the state 101, the next state will be:
   a) 011 b) 100 c) 000 d) 010 e) None of these
2) Consider the counter in (**point '**), The number of stuck states is:
   a) 3 b) 2 c) 1 d) Zero e) None of these
3) Consider the counter in (**point '**), If the counter goes to the state 111, the next state will be:
   a) 000 b) 100 c) 001 d) 010 e) None of these
4) Consider the counter in (**point '**), the input of the first flip-flop A is
   a) $D_A= B'.C$ b) $D_A=B$ c) $D_A=A.C$ d) $D_A=C$ e) None of these
5) Consider the counter in (**'**), the input of the second flip-flop B is
   a) $D_B=A.C$ b) $D_B=C$ c) $D_B=A'.C$ d) $D_B=A$ e) None of these
6) Consider the counter in (**point '**), the input of the third flip-flop C is
   a) $D_C=A.B$ b) $D_C=A$ c) $D_C=B.C$ d) $D_C=C'$ e) None of these

**Taking into consideration the algorithmic state machines chart shown in figure, solve the questions from (point 7) to (point 10)**



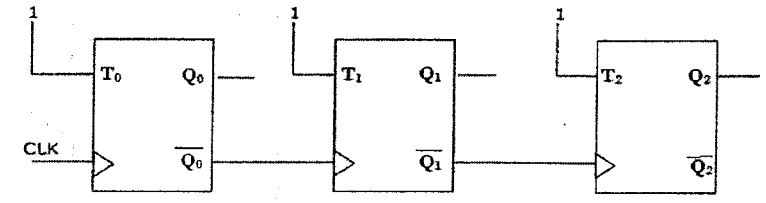

7) How many states in the chart?
   a) 2 b) 3 c) 4 d) 6 e) None of these
8) How many blocks in the chart?
   a) 6 b) 4 c) 3 d) 2 e) None of these
9) How many inputs are required for the control logic part?
   a) 6 b) 4 c) 3 d) 2 e) None of these
10) What is the minimum number of flip-flops needed to build the control logic part?
   a) 4 b) 3 c) 2 d) 1 e) None of these

11) The terminal count of a modulus-11 binary counter is _____.
   a) 1010 b) 1011 c) 1001 d) 1100 e) None of these
12) Mealy machine has _____ states than a Moore machine.
   a) Fewer b) More c) Equal d) Negligible e) None of these
13) Conditional box has a shape of
   a) square b) rectangle c) oval d) pentagon e) None of these
14) What is a square wave generator?
   a)Bistable multivibrator b)Astable multivibrator c)Monostable multivibrator d) None of these
15) ……. is useful for creating a timing period of fixed duration in response to some external event.
   a) Astable Multivibrator b) Monostable Multivibrator c) Bistable Multivibrator d)None of these
16) Which of the following conditions must be met to avoid race around problem.
   a) Pulse width < Propagation delay b) Pulse width >Propagation delay c) None of these

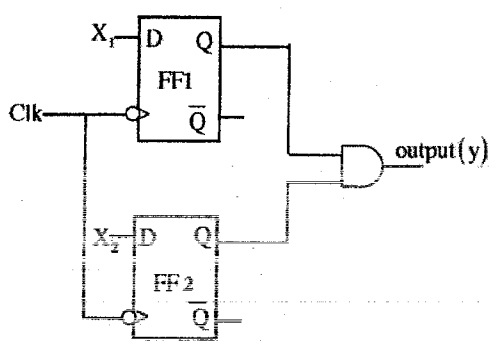


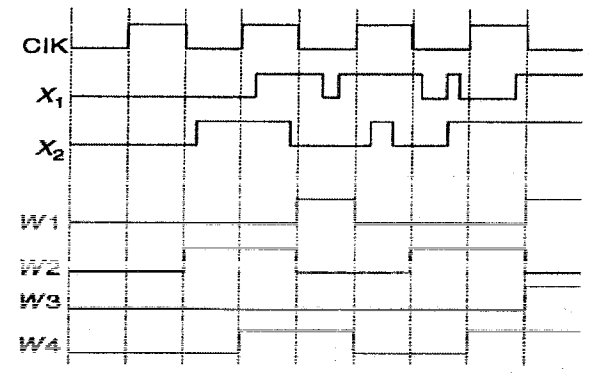


17) A MOD-5 ripple counter uses a flip-flop with propagation delay of 20 ns. The pulse width of strobe is 30ns. The frequency of input signal which can be used for proper operation of counter is?
   a) 8 MHz b) 13 MHz c) 20 MHz d) 22 MHz e) None of these
18) For a MOD-12 ripple counter, the flip-flop has a propagation delay = 60 ns and the NAND gate has a propagation delay of 25 n sec. The max. clock frequency that can be used is equal to
   a) 3.77 MHz b) 4.87 MHz c) 1.34 MHz d) None of these
19) The given figure shows a ripple counter using positive edge triggered flip flops. If the present state of the counter is $Q_0\ Q_1\ Q_2 = 110$, then its next state $Q_0\ Q_1\ Q_2$ will be



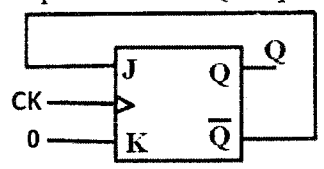

   a) 010 b) 001 c) 111 d) 101 e) None of these
20) Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is:
   a) 0, 1, 3, 7, 15, 14, 12, 8, 0 b) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
   c) 0, 8, 12, 6, 8, 10, 12, 1, 0 d) 0, 8, 12, 14, 15, 7, 3, 1, 0 e) None of these
21) Asynchronous counters eliminate the ……. problems encountered with synchronous counters.
   a) delay b) stuck c) race around d) None of these
22) The minimum number of D flip-flops needed to design a mod-258 counter is.
   a) 9 b) 8 c) 7 d) 258 e) None of these
23) Three cascaded D flip-flop will divide the input frequency by _____.
   a) 3 b) 6 c) 8 d) None of these
24) Race around problem is unwanted and uncontrollable oscillations occurring in ……..
   a) Pulse-triggered JK b) Edge-triggered JK c) All of these d) None of these
25) The state diagram to describe a sequence detector using a Moore machine that detects three consecutive 0's or three consecutive 1's with overlapping includes at maximum:
   a) 4 states b) 5 states c) 6 states d) 7 states e) None of These
26) A sequence detector is designed to detect precisely 3 digital inputs, without overlapping sequences detectable. For the sequence (1X1) and input data (110101001111010): what is the output of this detector?
   a) 000101000011110 b) 000101000010110 c) 000001000010010 d) None of These
27) In the circuit shown, choose the correct timing diagram of the output (y) from the given waveforms W1, W2, W3 and W4.




   a) W1 b) W2 c) W3 d) W4 e) None of these
28) A sequence detector using a Mealy machine is required to give a logical output of 1 whenever the sequence 11010001 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is
   a) 8 b) 5 c) 4 d) 3 e) None of These

29) In a JK flip-flop, we have J=Q' and K=0 (see figure). Assuming the flip-flop was initially with Q=1 and then clocked for 6 pulses, the next sequence at the Q output will be




a) 101010 b) 000000 c) 111111 d) 010101 e) None of these

30) Assume that a four-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the four-bit pattern after the fourth clock pulse? (Right-most bit first.)
a) 1111 b) 1100 c) 0000 d) 0011 e) None of these

31) In a 3-bit Johnson counter sequence, there are a total of how many states or bit patterns?
a) 6 b) 8 c) 3 d) 10 e) None of these

32) The state diagram to describe a sequence detector using a Moore machine that accept a string containing even number of zeros:
a) 2 states b) 3 states c) 4 states d) 5 states e) None of These

33) The output of a 5-input AND gate is connected to the input of 2 gates, this gate has a fan-out of……
a) 2 b) 3 c) 4 d) 5 e) None of the mentioned

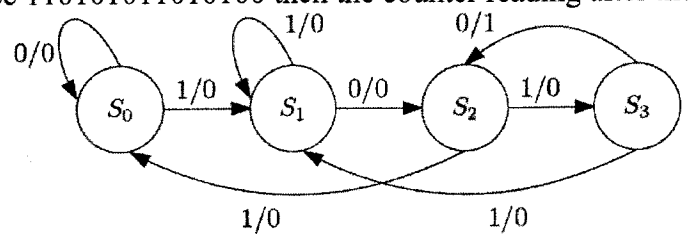
34) The output of a 2-input AND gate is connected to the input of 5 gates, this gate has a fan-in of ……
a) 2 b) 3 c) 4 d) 5 e) None of the mentioned

35) How many pulses are needed to change the contents of a 4-bit down counter from 1100 to 0111 (rightmost bit is the LSB)?
a) 4 b) 5 c) 6 d) 7 e) None of these

36) The number of unused states in the 6-bit Johnson counter is:
a) 6 states b) 32 states c) 64 states d) None of these

37) Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-$2^n$ bit decoder. This circuit is equivalent to a ……..
a) k-bit ring counter. b) 2k-bit ring counter. c) k-bit Johnson counter. d) None of these

38) The given figure shows the state graph of a sequence detector machine. The output of machine is connected to a decimal counter that increments whenever the output goes high. If the input to the machine is the sequence 110101011010100 then the counter reading after the end of sequence is



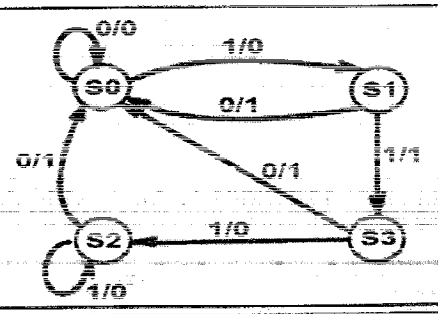

a) 2 b) 3 c) 4 d) 5 e) None of these

39) A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is…
a) constantly LOW b) constantly HIGH
c) a 20 kHz square wave d) a 10 kHz square wave e) None of these

40) An 8-bit serial in/serial out shift register is used with a clock frequency of 200 kHz to achieve a time delay (td) of _____
a) 5 µs b) 10 µs c) 20 µs d) 40 µs e) None of these

41) What is the number of states obtained after minimizing the given state graph shown in figure?
a) 2 b) 3 c) 4 d) None of these

42) Consider the state graph in (**point 41**), what is the minimum number of flip-flops needed to build the equivalent circuit for the state graph after minimization?
a) 1 b) 2 c) 3 d) 4 e) None of these







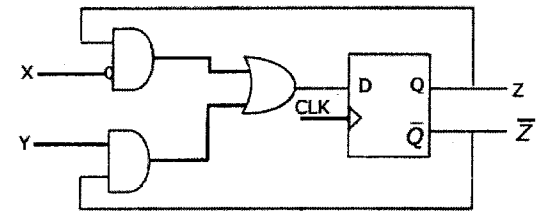

43) To convert D flip-flop to JK flip-flop:
a) D=J'.Q+Q'.K b) D= J.Q'+Q'.K c) D= J.Q'+Q.K' d) None of these

44) Assume a 4-bit ripple counter has a failure in the second flip-flop such that it "locks up". The third and fourth stages will _____
a) Continue to count with correct outputs b) Turn into molten silicon
c) Continue to count but have incorrect outputs d) Stop counting e) None of these

45) In DOWN-counter, each flip-flop is triggered by the …….. of the preceding flip-flop
a) inverted output (Q') b) output (Q) c) input d) None of these

46) In asynchronous circuit, the changes occur with the change of
a) input b) output c) clock pulse d) time e) None of these

47) A sequential circuit using D flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is




a) S–R Flip-Flop with inputs X = R, Y = S b) J–K Flip-Flop with inputs X = S, Y = R
c) J–K Flip-Flop with inputs X = K, Y = J d) None of these

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